A Model & Design Methodology for Dead Time Linearised Current Controlled Ring Oscillator ADCs

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***Abstract*—The Current Controlled Ring Oscillator's (CCRO) non-linear characteristic, has limited its performance in ADCs and the lack of an analytical model for this non-linearity has slowed its adoption. Previously published work has constrained CCRO non-linearity to a dead time. In this work, we present a model for understanding the dynamic performance of that linearised CCRO using its dead time. We also present a systematic CCRO design methodology to demonstrate the trade-offs required to achieve a specified performance, allowing designers to evaluate potential ADC performance before the schematic design stage. The model is validated using measured results from a CCRO-based current-domain ADC with** 50 dB **SNDR at** 1 MHz **NBW in 65nm CMOS.**

***Index Terms*—CCRO, Design Methodology, Linearisation, VCO based ADC, Ring Oscillator, Modelling**

I. Introduction

TECHNOLOGY nodes scaling to ever smaller dimensions results in lower gain transistors and reduced supply headroom, making it more difficult to create ADCs with the specifications demanded by modern applications. While dynamic range is limited in the voltage domain as supply headrooom shrinks, time-domain resolution improves as devices get faster. The Current Controlled Ring Oscillator (CCRO) is a current-to-frequency (or time) transducer; it takes advantage of advanced processes, such as decreased gate delay, and avoids their drawbacks, such as reduced supply voltage.

The CCRO is a non-linear element; which has limited its performance in ADCs, with many techniques being employed to improve its performance. Calibration using inverse polynomials and lookup-tables [1], [2] corrects non-linearity, but at the cost of increased complexity and power consumption. Using closed-loop feedback, [3] also improves performance, but at the cost of reduced input bandwidth. A number of circuit compensation techniques are employed by using resistors [4], [5] or g_m elements [6] but their reliance on two non-linearities cancelling leads to concerns about robustness to mismatch.

Prior works have reduced the inherent non-linearity of the CCRO by reducing the ratio of delay cell discharge time to their charge time [7], [8]. Our previous work [9] has improved on this architecture by constraining the CCRO non-linearity to a constant dead time, t_{dead}, improving both the magnitude of the non-linearity ($HD2$ improved by 10 dB), and the predictability of the non-linearity by removing strong PVT dependence. Although this technique has been successfully implemented, a link between t_{dead} and dynamic performance has not been published, nor has a systematic design methodology for the topology.

The remainder of this paper is structured as follows: Sec. II presents a model for CCRO non-linearity based on dead time and discusses quantisation noise in terms of dead time, Sec. III shows the tradeoff between quantisation noise and linearity, and presents a systematic design methodology. Finally, Sec. IV provides measurement results to validate the presented models, and Sec. V concludes the paper.

II. The Dead Time Model

A. Deriving the Current-to-Frequency Characteristic

Our previous work, [9], has implemented a CCRO (Fig. 1) which uses an inverter (M_{B0}) with a switching threshold independent of input current (I_{IN}) and positive feedback transistor (M_{FB0}) to stabilise the cell threshold, V_{TH} (that of the M_B inverter, e. g. M_{B0} of Fig 1a). The M_{C0} inverter provides a rail-rail drive to the next stage (as shown in the Φ_{OUT} traces of Fig. 1b), ensuring consistent load capacitance, C_L, discharge via M_{NA0}, irrespective of input current. These implementations result in the non-linearities of the oscillator being constrained to a constant dead-time equal to:

$$t_{dead} = Nt_{dead}^{cell} = N\left(t_{f,B} + t_{r,C} + t_{disch,A} + t_{r,B} + t_{f,C}\right) , \tag{1}$$

with N the number of delay cells in the ring, t_r and t_f the rise and fall time of the respective squaring inverter, and $t_{disch,A}$ the discharge time of the main inverter. A CCRO frequency results:

$$f_{CCRO}(t) = \frac{1}{T_{CCRO}} = \frac{1}{NC_LV_{TH}/I_{IN}(t) + t_{dead}} , \tag{2}$$

Previous works [7], [8] reach an equation of the same form, but explicitly describe t_{dead} as a function of discharge current of the main inverter and ignore the contributions from the squaring inverters. (2) shows that t_{dead} contributes to the non-linearity of the CCRO, and the limit $t_{dead} \to 0$ yields a linear CCRO. Reducing t_{dead} requires M_{NA0} to become larger for a faster discharge, which increases the size of M_{C0} to drive it, and of M_{B0} to drive that; all increasing power consumption. It is important to quantify the effect t_{dead} has on linearity, and to optimise it considering the system specifications. The time a delay cell spends charging, t_{active}, is given by:

$$t_{active}(I_{IN}) = \frac{NC_LV_{TH}}{I_{IN}} = \frac{1}{K_{CCRO}I_{IN}} , \tag{3}$$

where $K_{CCRO} = 1/NC_LV_{TH}$, then the $t_{active} : t_{dead}$ ratio (TADR) is:

$$TADR(I_{IN}) = \frac{t_{active}(I_{IN})}{t_{dead}} = \frac{1}{K_{CCRO}I_{IN}t_{dead}} . \tag{4}$$

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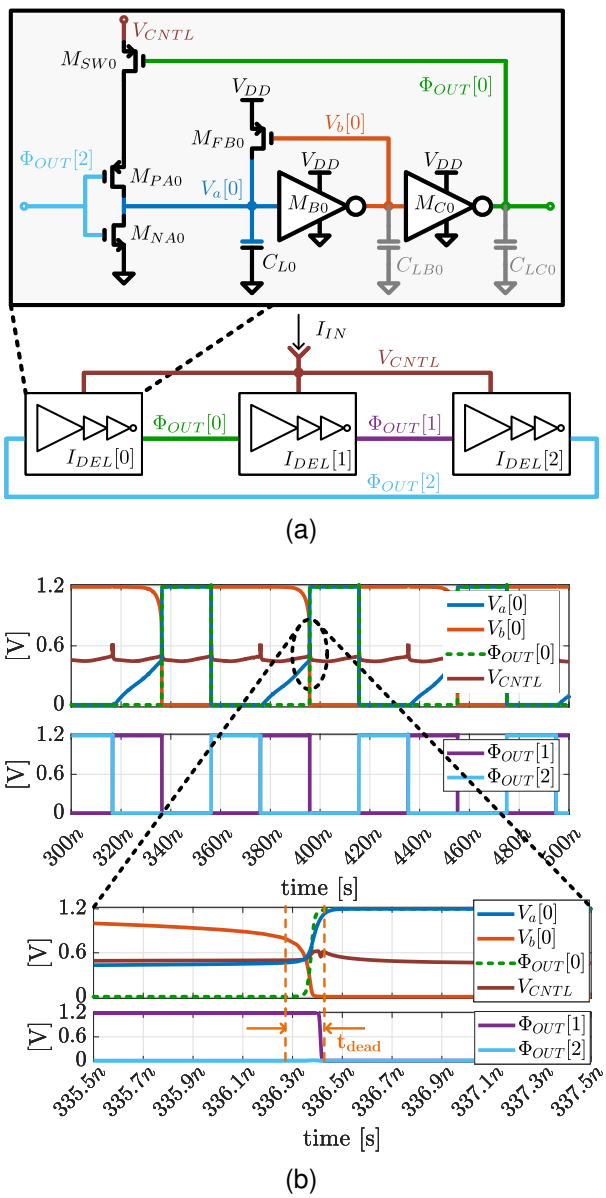


Fig. 1. (a) Schematic and (b) Associated waveforms of the CCRO.

The frequency can thus be re-written in terms of TADR:

$$f_{CCRO}(I_{IN}) = \frac{1}{t_{active} + t_{dead}} = \frac{1}{t_{active}\left(1 + \frac{1}{TADR}\right)} . \quad (5)$$

$f_{CCRO}(I_{IN})$ is not a polynomial, so a Taylor series is used to quantify its non-linear components. The input current consists of a bias and a time-varying component, $I_{IN}(t) = I_{BIAS} + i_{in}(t)$, and for maximum accuracy, the Taylor series should be taken about I_{BIAS}. This greatly complicates the resulting equations and obscures the intuition that flows from them. A sufficiently accurate approximation for the Taylor series is given by the Maclaurin series by setting $I_{BIAS} = 0$:

$$f_{CCRO}(I_{IN}) \simeq \frac{1}{t_{active}} + \frac{1}{TADR\ t_{active}} + \frac{1}{TADR^2\ t_{active}} \quad (6)$$

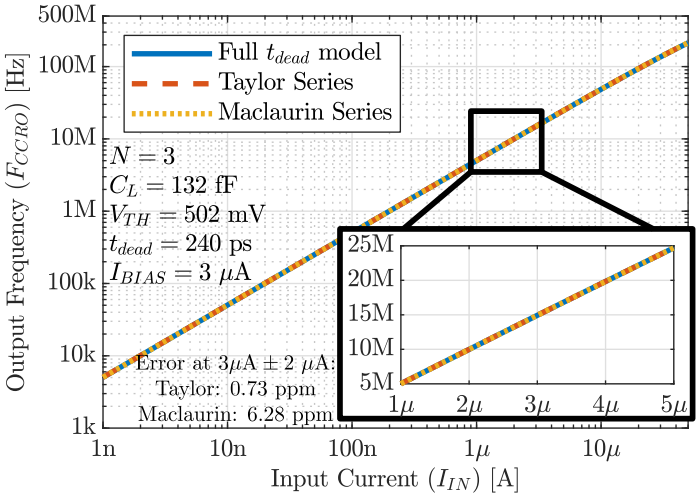


Fig. 2. Comparison between t_{dead} model and approximations.

Fig. 2 plots the true $f_{CCRO}(I_{IN})$, the 3rd order Taylor and Maclaurin approximations for a typical CCRO, showing $<$ 10 ppm error for both approximations. The full Taylor series can be calculated using symbolic maths packages. (6) shows the 2nd order term is proportional to TADR, the 3rd order term to TADR^2

B. Calculating Harmonic Distortion

The polynomial expression of (6) allows the harmonic distortion of the CCRO to be estimated. Assuming a sinusoidal input $i_{in}(t) = I_{in}^{pk} \cos(2\pi f_{in} t)$, the resultant output is:

$$f_{CCRO}(t) = \frac{1}{t_{active}}\left(1 + \frac{3}{4TADR^2}\right) \cos(2\pi f_{in} t) \quad (7)$$

$$+ \frac{1}{2TADR\ t_{active}} \cos(2\pi 2 f_{in} t) \quad (8)$$

$$+ \frac{1}{4TADR^2\ t_{active}} \cos(2\pi 3 f_{in} t) \quad (9)$$

From this, the harmonic distortion terms can be calculated:

$$HD2 = \frac{H_2}{H_1} = \frac{1}{2TADR\left(1 + \frac{3}{4TADR^2}\right)} \simeq \frac{1}{2TADR} \quad (10)$$

$$HD3 = \frac{H_3}{H_1} = \frac{1}{4TADR^2\left(1 + \frac{3}{4TADR^2}\right)} \simeq \frac{1}{4TADR^2} \quad (11)$$

where H_k is the kth harmonic amplitude and HDk the kth distortion term. $HD2$ increases at 20 dB/dec of input current, while $HD3$ increases at 40 dB/dec. When correctly designed, $TADR >> 1$ ($\sim$ 105 at the bias point in [9]), so that $HD2$ dominates. Fig. 3 plots (10) and (11), showing the harmonic distiortion for a given $TADR$ and thus I_{IN}^{pk}.

C. Linking Quantisation Noise to TADR

It appears the SNDR can be arbitrarily improved by decreasing K_{CCRO} to increase TADR, but K_{CCRO} also determines the input-referred quantisation noise. Take the RMS quantisation error in the Nyquist band to be $\Delta/\sqrt{12F_s}$, where F_s is the ADC sampling rate and $\Delta = 2\pi/N$, the phase quantisation step of the CCRO. The input-referred quantisation noise current density is:

$$\overline{i_{nq}}(f) = \frac{\pi f}{\sqrt{3} N K_{CCRO} \sqrt{F_s}} = \frac{\pi f\ TADR\ t_{dead}\ I_{IN}^{pk}}{\sqrt{3} N \sqrt{F_s}} \quad (12)$$

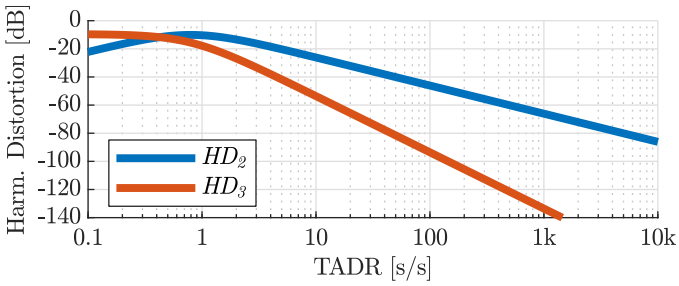


Fig. 3. Plot of HD2 and HD3 vs. TADR.

using (4) to obtain the expression in terms of $TADR$. The frequency dependence of $\overline{i_{nq}}$ is due to CCRO ADC first order noise shaping. Integrating $\overline{i_{nq}}(f)$ to the noise bandwidth (NBW) of the ADC yields:

$$i_{nq}(NBW) = \frac{\pi\ TADR\ t_{dead}\ I_{IN}^{pk}\ NBW^{\frac{3}{2}}}{3N\sqrt{F_s}} \tag{13}$$

An expression for the SQNR of the ADC can be obtained:

$$\begin{aligned} SQNR &= 20\log_{10}\left(\frac{I_{IN}^{pk}}{\sqrt{2}\ i_{nq}(NBW)}\right) \\ &= 20\log_{10}\left(\frac{3}{\sqrt{2}}\frac{N\sqrt{F_s}}{\pi\ TADR\ t_{dead}\ NBW^{\frac{3}{2}}}\right)\ [\text{dB}]\ , \end{aligned} \tag{14}$$

assuming a sinusoidal input of amplitude I_{IN}^{pk} and white quantisation noise, a simplified approximation [10], but one suitable for initial design exploration. In reality, the CCRO is a pulse-frequency modulator (PFM), and tones at the oscillator free running frequency can alias in-band. It can be seen from (14) that SQNR is inversely proportional to $TADR$, while harmonic distortion improves with $TADR$ (10). This poses a direct trade-off between quantisation noise and linearity.

III. A CCRO Design Methodology

A. The Quantisation-Linearity Tradeoff

The above trade-off ensures that the *peak* SNDR obtainable does not depend on K_{CCRO} (thus C_L). This is illustrated in Fig. 4 by sweeping C_L from 5 fF to 1 pF changing K_{CCRO}; the same peak SNDR is obtained, albeit shifted. When the same curves are instead plotted against $TADR$ on the x-axis, as in Fig. 5, it is clear that peak SNDR occurs at the same $TADR$ for all K_{CCRO}. $TADR_{pk}$, the point of peak SNDR, is the value of $TADR$ when SNQR (14) and harmonic distortion (10) are equal. $TADR_{pk}$ is:

$$TADR_{pk} = \sqrt{\sqrt{\frac{9}{8}}\frac{N\sqrt{F_s}}{\pi\ t_{dead}\ NBW^{\frac{3}{2}}}} \tag{15}$$

Thus, the peak SNDR point is given by noting that when harmonic distortion (HD2) equals SQNR, the SNDR is 3 dB below either of them:

$$SNDR_{pk} = \frac{2\ TADR_{pk}}{\sqrt{2}} = \sqrt{\sqrt{\frac{9}{2}}\frac{N\sqrt{F_s}}{\pi\ t_{dead}\ NBW^{\frac{3}{2}}}} \tag{16}$$

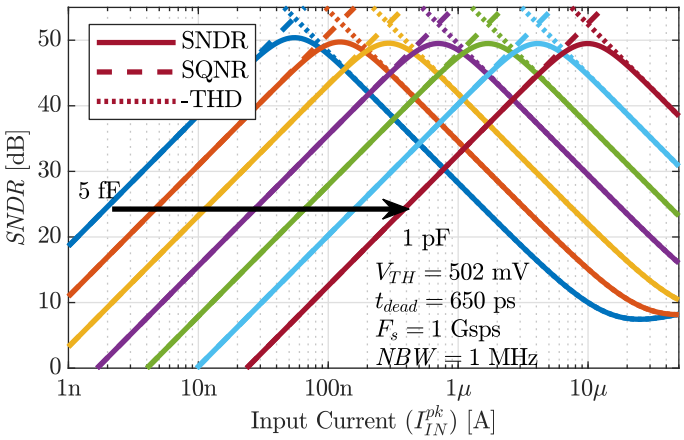


Fig. 4. Plot of SNDR vs. input current for a range of C_L.

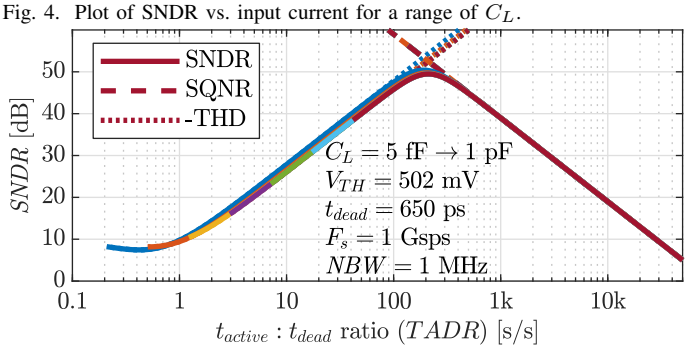


Fig. 5. Plot of SNDR vs. $TADR$ for a range of C_L.

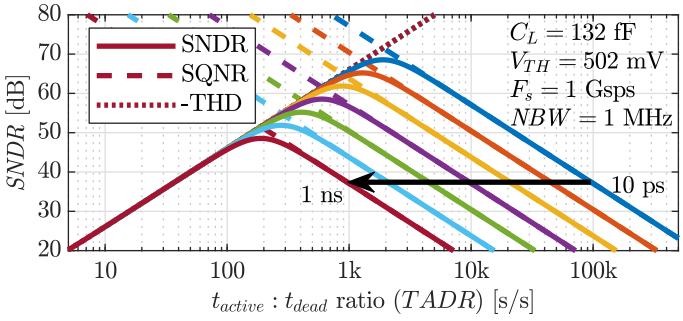


Fig. 6. Plot of SNDR vs. $TADR$ for a range of t_{dead}.

B. Design Methodology

$t_{dead} \propto N$, as in (1), since it refers to the total dead time around the ring, so changing N has no effect on SNDR^{pk}. (16) shows that for a fixed F_S and NBW, the only way to improve peak SNDR is to decrease t_{dead}, shown by Fig. 6 plotting SNDR and sweeping t_{dead} logarithmically from 10 ps to 1 ns. To achieve a required peak SNDR, the minimum t_{dead} required should be chosen, assuming fixed F_s and NBW, as in Fig. 7. The choice of t_{dead} will have process technology implications, and reducing t_{dead} will invariably increase power consumption. The design of [9] required $SNDR = 50$ dB, thus $t_{dead} < 700$ ps. Calculate $TADR_{pk}$ and use (4) to choose K_{CCRO} to yield SNDR^{pk} at the desired I_{IN}^{pk}. [9] required $< 1\ \text{nA}_{\text{rms}}$ noise, allowing 3 μA bias current, so $I_{IN}^{pk} = 1\ \mu$A was chosen. Lastly, size C_L to give the required K_{CCRO} using (3). Dead time model CCROs, such as [9] consume most of their power to limit t_{dead}, so are assumed quantisation noise limited. The analysis presented assumes this, ignoring CCRO

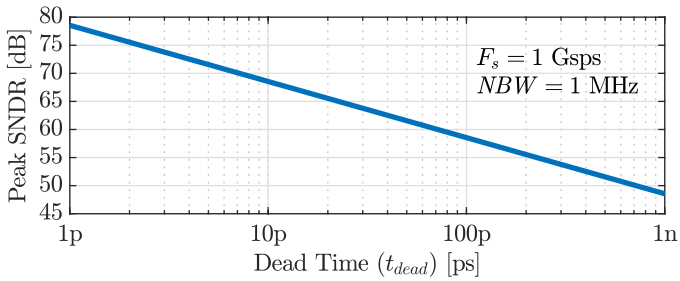


Fig. 7. Plot of peak SNDR vs. t_{dead}.

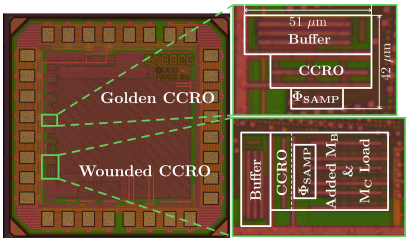


Fig. 8. Die Micrograph showing Golden and Wounded Channels.

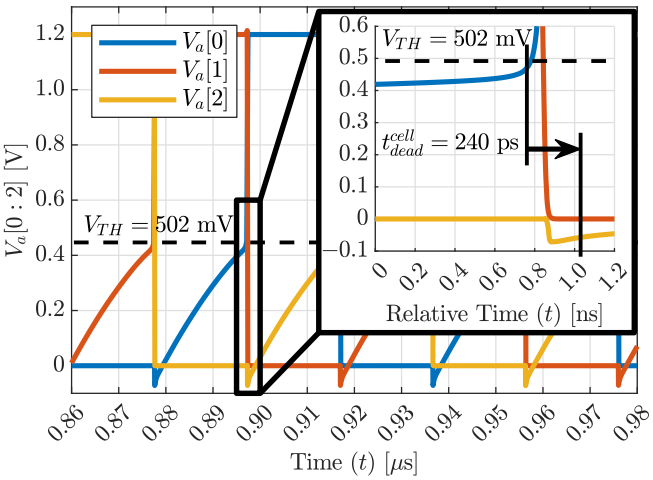
bias current thermal noise. There is freedom in the choice of bias current, which sets the free-running f_{CCRO}.

IV. Measurement Results

Two CCRO designs were implemented on the IC presented in [9] (die micrograph shown in Fig. 8) to validate the TADR model; the golden circuit published in [9], and a wounded circuit with reduced C_L and increased t_{dead} (realised by increasing the parasitic C_{LB} and C_{LC} shown in Fig. 1a). The model is validated by first observing t_{dead}, C_L and V_{TH} in time-domain extracted simulations, creating a transfer characteristic using (6), and comparing this transfer characteristic to the observed one, both in simulation and measured data. The SNDR across I_{IN} is then calculated using (10, 11), (14) and taking into account thermal noise contributed by I_{BIAS}.

Fig. 9a shows $t_{dead}^{cell} = 240$ ps, $V_{TH} = 502$ mV and $C_L = 132$ fF for the golden CCRO simulation. Fig.9b shows $t_{dead}^{cell} = 420$ ps for the wounded CCRO simulation, with $V_{TH} = 502$ mV also, but $C_L = 48$ fF. TADR models of both CCROs were constructed from these parameters, which were compared with both simulation and measured results in Fig. 10. The simulated frequency characteristics of both the golden and wounded CCRO are in excellent agreement with the TADR model derived from the time-domain waveforms.

The TADR model predicts peak SNDR and the input current it occurs at. This is demonstrated by performing dynamic tests on the CCRO sampled output (sampler from [9]). The input amplitude, I_{IN}^{pk}, is swept and an FFT taken at each point. A Representative FFT for the ADC is shown in [9]. The SNDR calculated from these FFTs is plotted on the dynamic range plots of Fig. 11. The TADR model (yellow) of the measured golden CCRO fits the measured (blue) SNDR excellently in Fig. 11a. Slight deviation to the predicted SNDR is seen at small amplitudes due to PFM tones, as described in [10], pushing quantisation noise to out-of-band tones. These tones can also alias in-band, and is the cause of the notch in the measured result at 1.2 μA. The position of these aliased tones is dependent on parasitics and bias current, so the simulation (orange) does not show the notches in the same locations



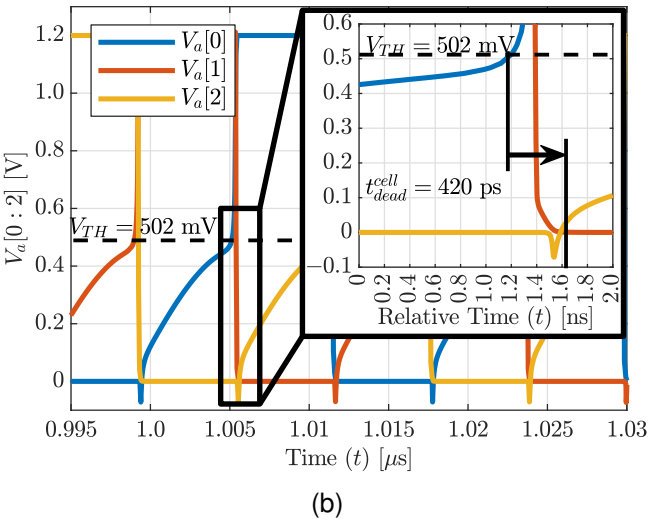


Fig. 9. Simulation waveforms showing the estimation of t_{dead} for a (a) golden and (b) wounded CCRO.

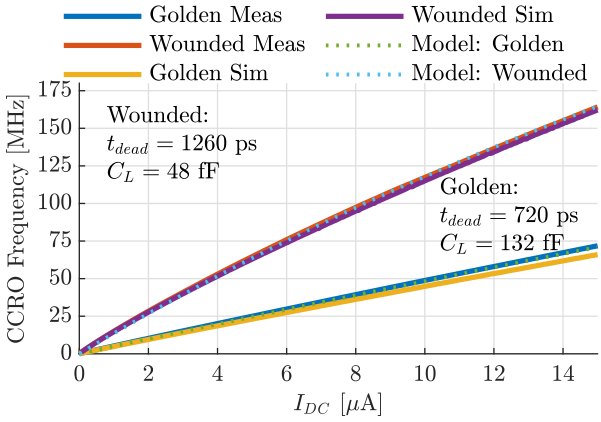


Fig. 10. Simulated & Measured CCRO Frequency Characteristics showing TADR model agreement.

as measured results. TADR accurately models SNDR up to 3 μA when the current buffer before the CCRO falls out of saturation and becomes highly non-linear. The wounded CCRO SNDR of Fig. 11b also matches the TADR model well. There is significant PFM tone aliasing at lower input levels [10], yielding a lower than predicted SNR, but the

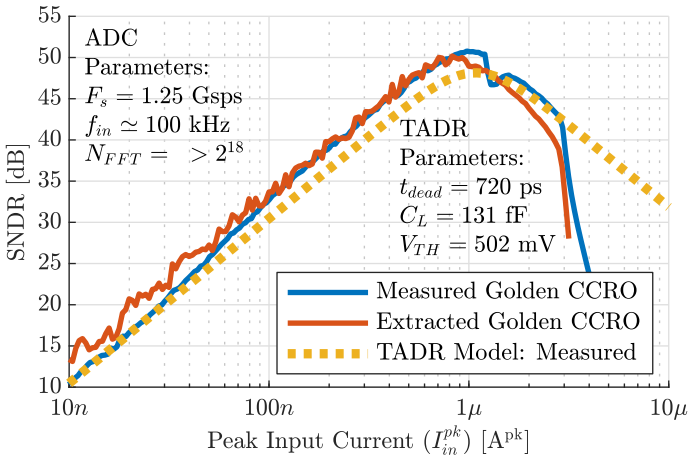


Fig. 11. Dynamic Measurements of the (a) golden and (b) wounded CCRO-based ADCs.

harmonic distortion prediction is accurate. To decouple the PFM aliasing from the expected SNDR, a noise-less simulation result is included; it shows PFM tones aliasing in and out of the signal band with notches in the SNDR. Without PFM aliasing, the SNDR matches the TADR model accurately, a limitation of using the white quantisation noise approximation in the TADR model.

V. Conclusion

A simple model is presented to predict the circuit-level requirements of a linearised CCRO-based ADC for a desired SNDR at a given input level. A direct link between the gate delay of a process (forming t_{dead}) and the achievable SNDR of a CCRO-based ADC is presented, proving that these architectures are inherently scaling friendly, in terms of both quantisation noise and linearity. Dead time linearised CCRO-based ADC designs have lacked a deterministic and simple model of non-linearity until now, limiting their adoption, particularly in industry. The model presented and its associated design methodology takes much of the guess-work out of linearised CCRO-based ADC design from a linearity and SNDR perspective. The model is distilled down to two main equations, (15) and (16), which, as validated by measured results, accurately predict linearised CCRO performance.

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