# **EE2013**

## **NON-LINEAR CIRCUIT ANALYSIS**

**LECTURE 15: BJT APPLICATIONS** 

Instructors: Alex Jaeger, Anthony Wall

Coordinator: Prof. Pádraig Cantillon-Murphy

# LECTURE SCHEDULE

Thursdays 11am-1pm (with short break)

Monday 9am-10am slot not used!

## LECTURE NOTES

https://www.jaeger.ie/ee2013/lec15 Uploaded after lecture takes place

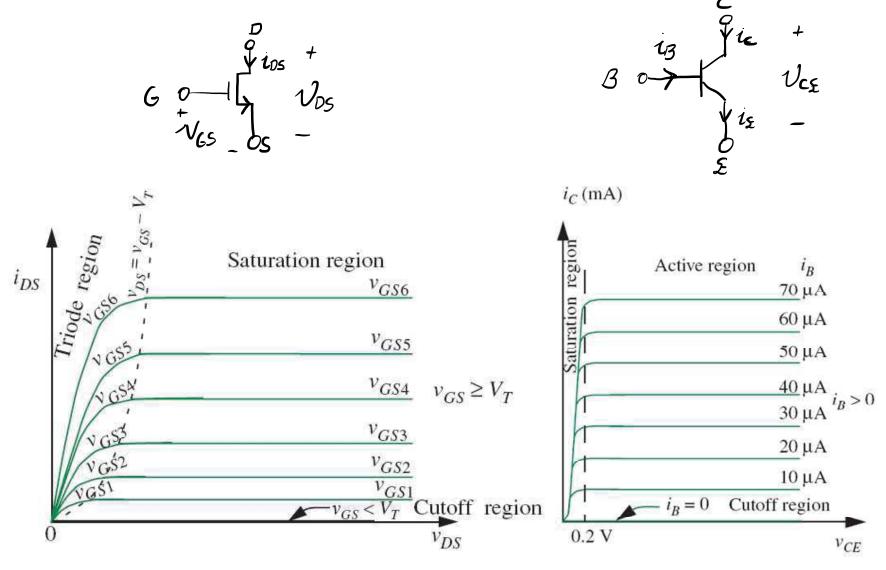
# **QUESTIONS?**

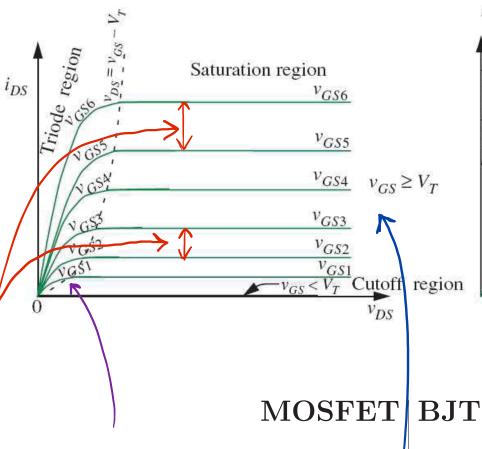
Just ask whenever it comes to you! OR:

anthony.wall@mcci.ie on Email, Teams or Canvas

### 1 Review from Last Time

### 1.1 Comparing the MOSFET and BJT

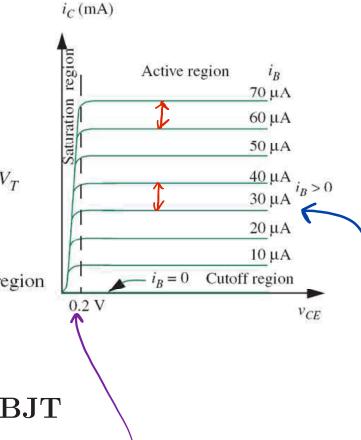




Saturation for  $v_{DS} > v_{GS} - V_T$  Forward active for  $v_{CE} > 0.2 \text{ V}$ 

$$i_{DS(sat)} = \frac{K}{2}(v_{GS} - V_T)^2 \left| i_C = \beta i_B \right|$$

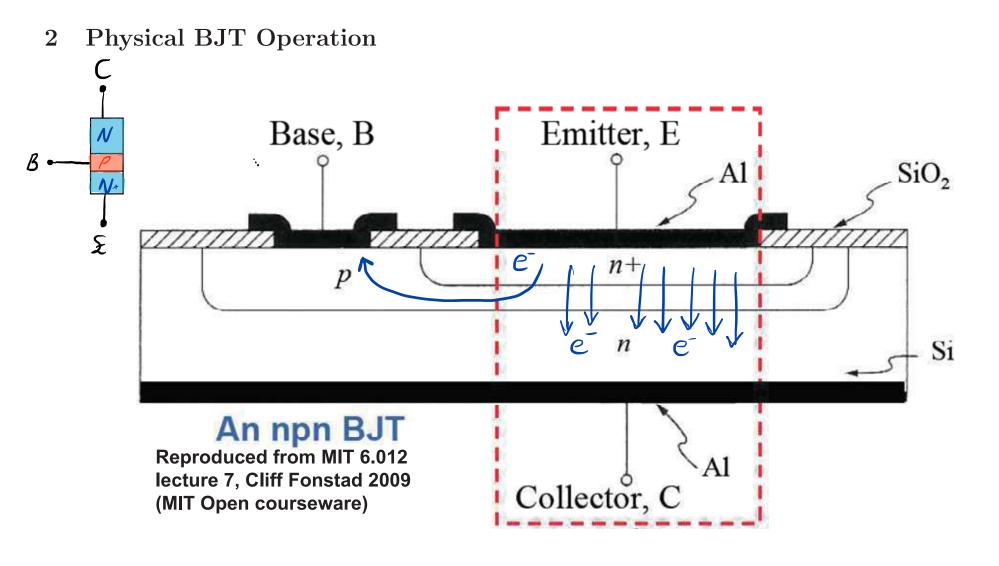
Voltage controlled current source | Current controlled current



$$i_C = \beta i_B$$
 \_\_\_\_

source

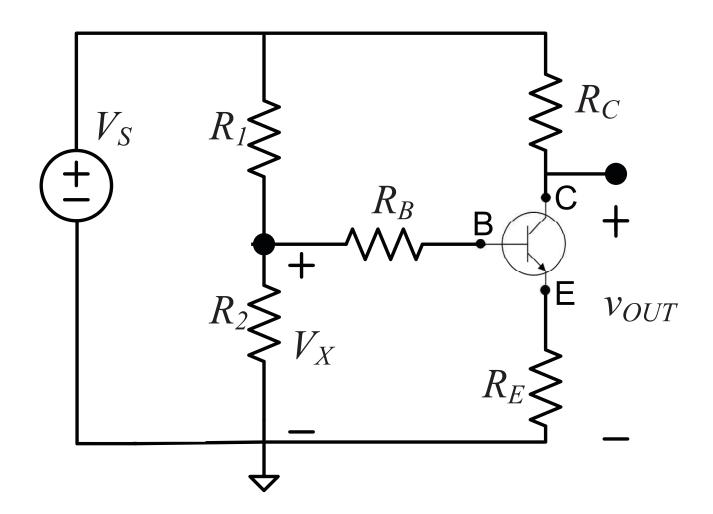
Non-linear device in saturation | Linear device in forward active



A typical NPN transistor comprises two semiconductor p-n junctions that share a thin p-doped 'sandwich.' In typical operation, the base-emitter junction is forward biased ( $v_{BE} \approx 0.6 \text{ V}$ ) so that thermally excited electrons are injected from the emitter into the base region. These electrons diffuse through the base from the region of high concentration near the emitter towards the region of low concentration near the collector. The collector-base junction is reverse-biased ( $v_{CB} < 0.4 \text{ V}$ ), and so little electron injection occurs from the collector to the base, but electrons that diffuse through the base towards the collector are swept into the collector by the electric field in the depletion region of the collector-base junction. It is this phenonomen that results in the large current gain, characterised by  $\beta$ , when the device operates in the forward active region.

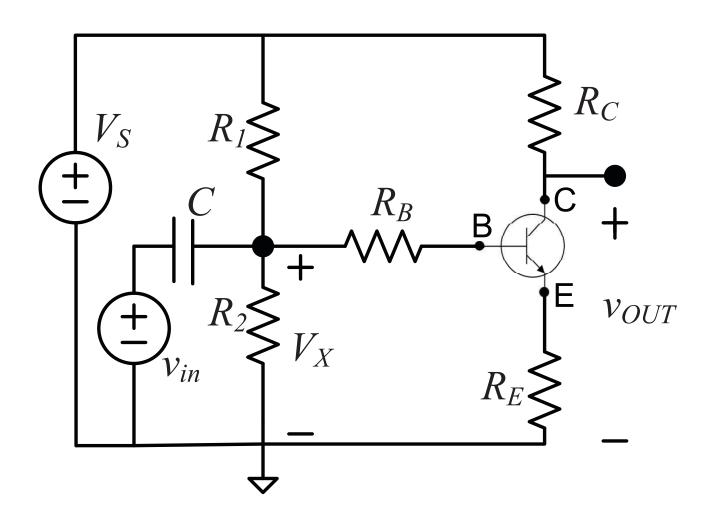
## 3 DC bias and the Common Emitter Amplifier

It is usual to ensure that the BJT operates in its forward active region by adding some *biasing* resistors at the input to ensure  $i_B > 0$ . Consider the circuit shown below with the biasing resistors,  $R_1$  and  $R_2$ .



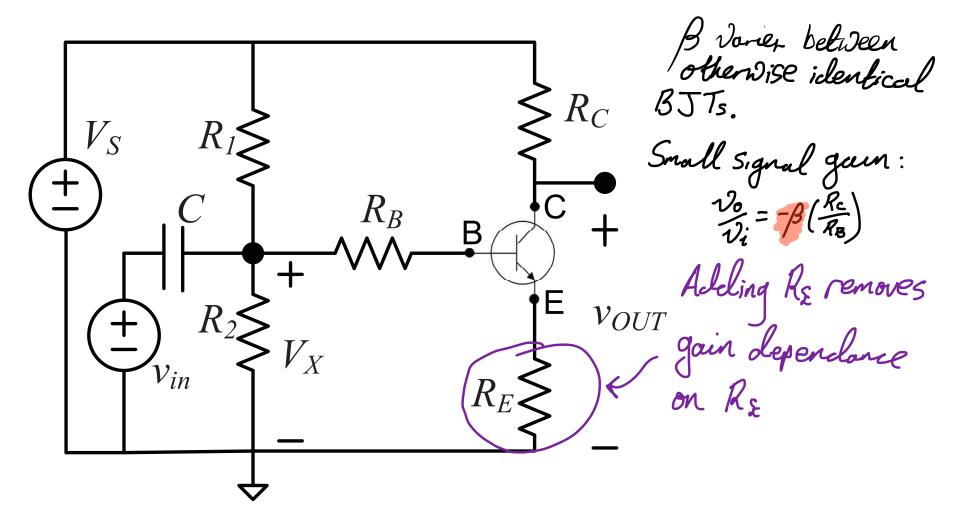
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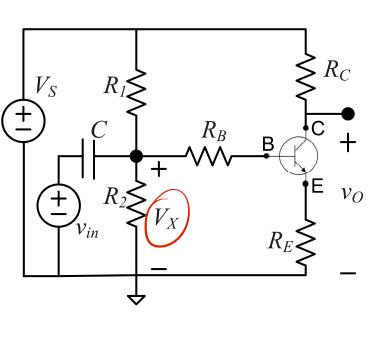


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In order to ensure that the bias resistor divider voltage  $(V_X)$  is not shorted to ground for large-signals (when  $v_{in} \to 0$ ), we need to add a blocking capacitor, C, which can be treated as an open circuit for DC signals and a short for small-signal analysis. The circuit also differs from that last lecture, due to the addition of the emitter resistance,  $R_E$ . We assume the DC voltage drop between the base and emitter is 0.6 V when the device operates in forward active mode.



#### 3.1 Large Signal (DC) Analysis

Consider the DC component of the output voltage,  $V_{OUT}$ :

$$I_{B} = \frac{V_{X} - V_{B}}{R_{B}} = \frac{V_{X} - (V_{\Sigma} + 0.6)}{R_{B}} = \frac{V_{X} - [(\beta + 1)I_{B}R_{\Sigma} + 0.6]}{R_{B}}$$

$$+ \frac{V_{X} - 0.6}{R_{B}} = \frac{V_{X} - 0.6}{R_{B}}$$

$$+ \frac{V_{X} - 0.6}{R_{B}} + (\beta + 1)R_{\Sigma}$$

In terms of IB: 
$$IB = \frac{V_x - 0.6}{R_B + (\beta + 1)R_E}$$

What if 
$$V_{x}$$
?

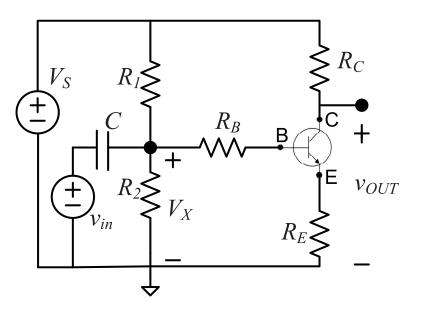
$$\frac{V_{s}}{R_{l}} \qquad KCL@V_{x}: \frac{V_{s}-V_{x}}{R_{l}} - \frac{V_{x}}{R_{2}} - \frac{V_{x}-(V_{E}+0.6)}{R_{B}} = 0$$

$$V_{x} = \frac{(V_{E}+0.6)R_{B}+V_{s}}{I+R_{l}(\frac{R_{B}R_{2}}{R_{B}+R_{2}})}$$

$$\int_{X} \begin{cases} \frac{R_{1}}{R_{2}} & R_{3} \\ R_{2} & V_{5} + 0.6V \end{cases} = \frac{\left(V_{5}\right)^{2}}{I}$$

$$V_{x} = \frac{(V_{\xi} + O V) RB + V3}{I + R_{I} \left(\frac{RB R_{2}}{RB + R_{2}}\right)}$$

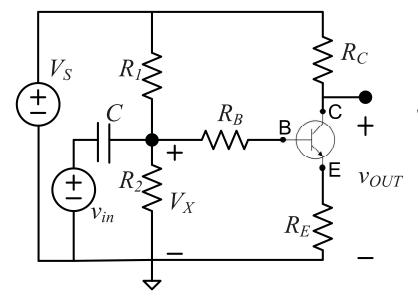
$$V_{x} \simeq \frac{V_{5} R_{2}}{R_{1} + R_{2}}$$
 When  $R_{B} \approx R_{1}$ ,  $R_{2}$ 



Consider the numerical quantities given here:  $R_B$  1k $\Omega$ ,  $R_C$  =  $10\mathrm{k}\Omega$ ,  $\beta$  = 100, and  $V_S$  = 10 V. Also, assume  $R_1$  6M $\Omega$ ,  $R_2$  =  $40\mathrm{k}\Omega$ , and  $R_E$  =  $10\mathrm{k}\Omega$ .  $R_3$  =  $100\mathrm{k}\Omega$ ,  $R_4$  =  $50\mathrm{k}\Omega$ ,  $R_2$  =  $50\mathrm{k}\Omega$ 

The DC base voltage,  $V_B$  is then calculated from  $I_B$ :

$$V_B = V_X - I_B R_B =$$

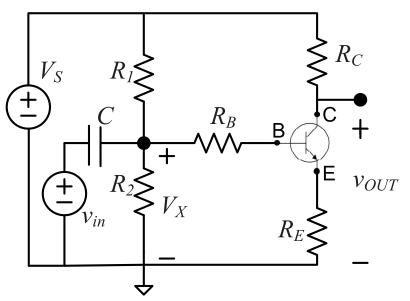


Consider the numerical quantities given here:  $R_B = 1 \text{k}\Omega$ ,  $R_C = 10 \text{k}\Omega$ ,  $\beta = 100$ , and  $V_S = 10$  V. Also, assume  $R_1 = 6 \text{M}\Omega$ ,  $R_2 = 4 \text{M}\Omega$ , and  $R_E = 10 \text{k}\Omega$ .  $R_3 = 100 \text{k}\Omega$ ,  $R_1 = 50 \text{k}\Omega$ 

$$V_{X} \simeq \frac{(10)(50k)}{50k + 50k} = 5V \qquad I_{B} = \frac{5 - 0.6}{(100k) + (100 + 1)(10k)} = 3.4 \mu A$$

The DC base voltage,  $V_B$  is then calculated from  $I_B$ :

$$V_B = V_X - I_B R_B = 5$$
 - (3.44)(100k) = 4.66 V



The DC base and emitter voltages only differ by the internal diode drop in forward active operation:

$$V_{\mathcal{L}} = V_{\mathcal{B}} - O \cdot 6 = 4 \cdot 06 V$$

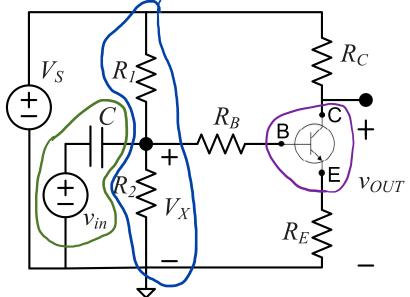
Therefore,  $V_{CE}$  is given by:

$$V_{CE} = V_{OUT} - V_E = [V_S - (\beta I_B)R_C] - V_E$$

$$= 10 - 100(344)(10k) - 4.06$$

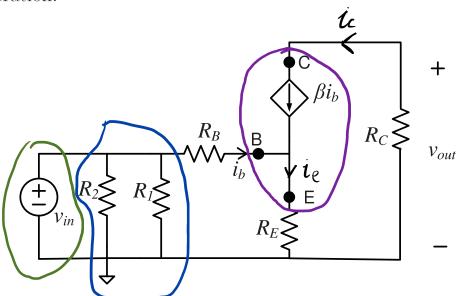
$$= 2.54V$$
forward
Adive Region

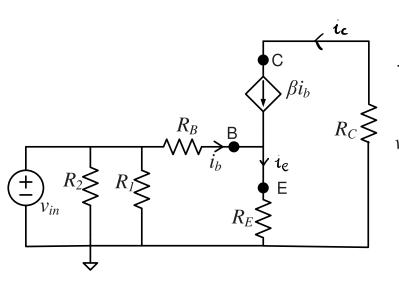
Clearly the condition for the device to operate in its forward active region ( $V_{CE} > 0.2 \text{ V}$ ) is satisfied.



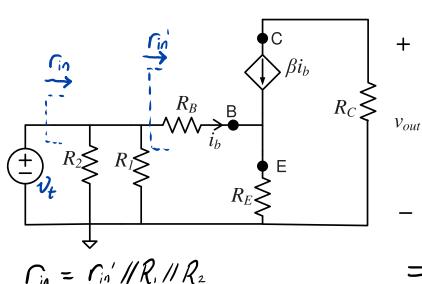
### 3.2 Small-signal Voltage Gain

To calculate the small-signal voltage gain,  $A_v$ , we set all DC voltage sources to zero (including the internal 0.6 V voltage drop from the base-emitter diode) and replace the capacitor with a short circuit. The BJT is replaced with its small-signal model in forward active operation.





$$\begin{array}{c|c}
 & I_b = \frac{\mathcal{V}_{in} - \mathcal{V}_e}{R_{\mathcal{B}}} = \frac{\mathcal{V}_{in}}{R_{\mathcal{B}}} - \frac{(\beta+1) \, l_b \, R_{\mathcal{S}}}{R_{\mathcal{B}}} \\
 & I_e \\
 & E \\
 & R_E \\
 & I_e \\
 & E \\
 & I_e \\
 & I_$$



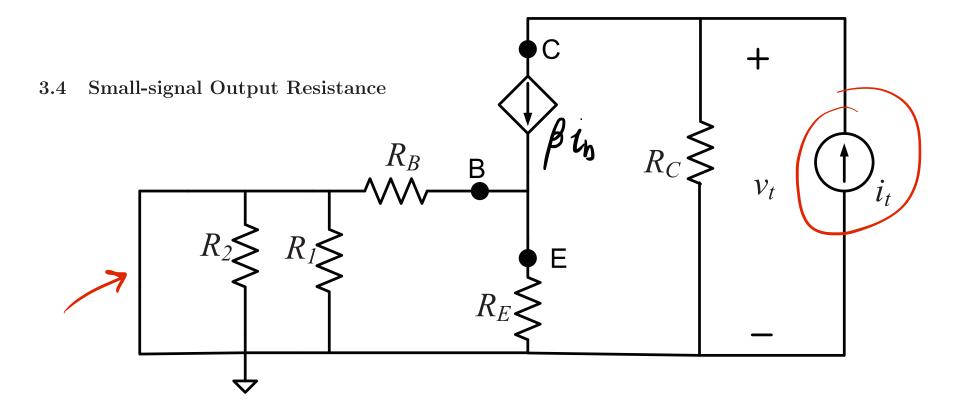
#### 3.3 Small-signal Input Resistance

To calculate the small-signal input resistance, we turn off  $v_{in}$  and apply a test source to the input.

To simplify this process, let's look beyond  $R_1$  and  $R_2$ , and consider the 'input resistance' looking into the base resistance,  $R_B$ . This new 'internal resistance,'  $r'_{in}$  appears in parallel with  $R_1$  and  $R_2$ .

$$\int_{a}^{b} i_{b} = R_{3} + (\beta+1)R_{2}$$

$$= 50k // 50// (100k + (101)(10k)) = 24.45 k \Omega$$



For the small-signal output resistance, we apply a test source at the output with  $v_{in} \to 0$ . Note that since the transistor is modeled by a small-signal current source, it is convenient to apply a test current source,  $i_t$ .

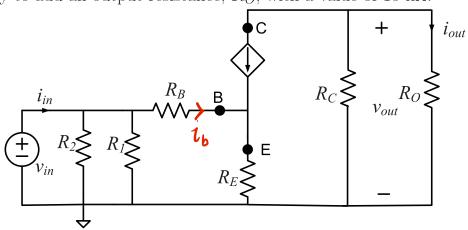
Furrent source, 
$$i_t$$
.

$$\int S_{ince} V_{in} = 0, \quad i_b = 0, \quad \beta c_b = 0$$

$$\int O = \frac{V_t}{i_t} = R_c = 10 \text{ k.l. here}$$

### 3.5 Small Signal Current Gain, $A_i$

To calculate the small-signal current gain,  $A_i = i_{out}/i_{in}$ , it is necessary to add an output resistance,  $R_O$ , with a value of 10 k $\Omega$ .



Fow much in maker it to is?

Lin [in' is Current]  $R_1/R_2$   $R_1/R_2$ 

= D.022

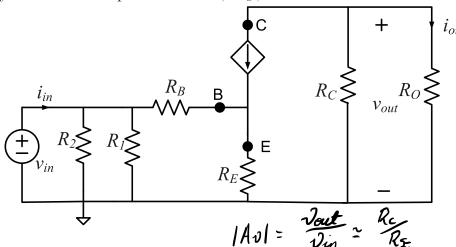
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How close tout relate to is? KCL@ Vout:

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What is the Current Gain?  $A_{i} = \frac{lout}{lin} = \frac{lout}{l_{b}} \cdot \frac{l_{b}}{lin}$   $A_{i} = \beta \left(\frac{R_{o}}{R_{c}+R_{o}}\right) \cdot \frac{(R_{c}//R_{2})}{\Gamma_{in}' + (R_{c}//R_{2})}$   $= (50)(O \cdot 022) = 1.1$ What is the Power Gain?  $A_{p} = |A_{v}| |A_{i}| = (1)(1.1)$