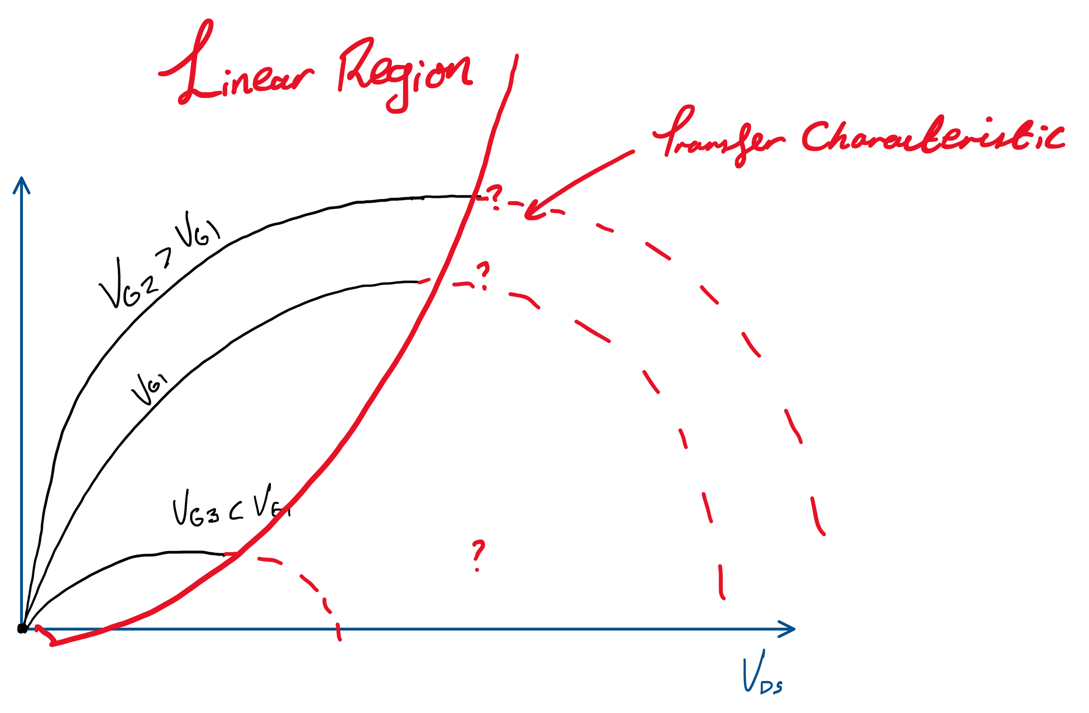
MOSFETs Part 11: Saturation

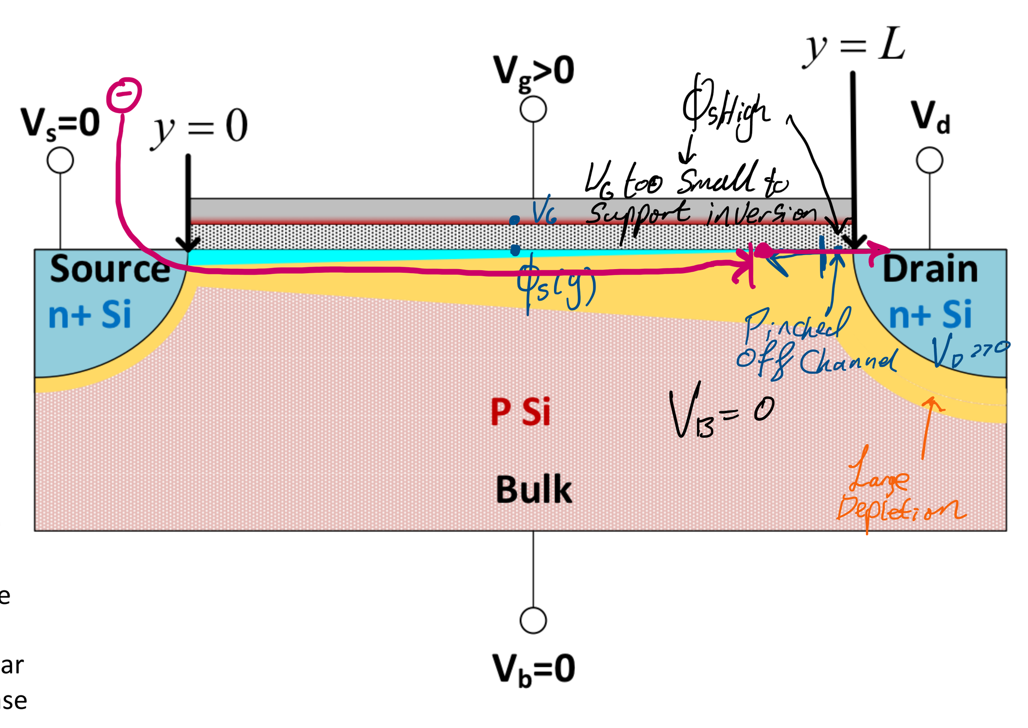
Tuesday 24 March 2020 09:54

- The previous section shows that for high V_{DS}, current will decrease
- This doesn't make sense
- Rather than the current starting to decrease, the device enters what is called the **saturation** region



Understanding the Saturation Region

- When the Drain Voltage V_D becomes large, the P-Bulk n+-drain P-N Junction becomes heavily reverse Biased
- A large Depletion region forms around the drain
- The Drain Voltage can become so large that the inversion charge is repelled
- This happens when the gate Voltage is no longer large enough to hold the inversion charge in place
- But if there's no inversion channel, how can current still flow?
  - Electrons are carried from the source through the channel to the end of the inversion channel
  - The electric field in this region is very high due to the high Drain Voltage
  - The distance between the end of the Channel and the drain is very small
  - The electrons are swept across the junction in a similar way to how minority carriers are swept across the base in a BJT



Mathematically Describing Saturation

- The Surface Potential is given by:

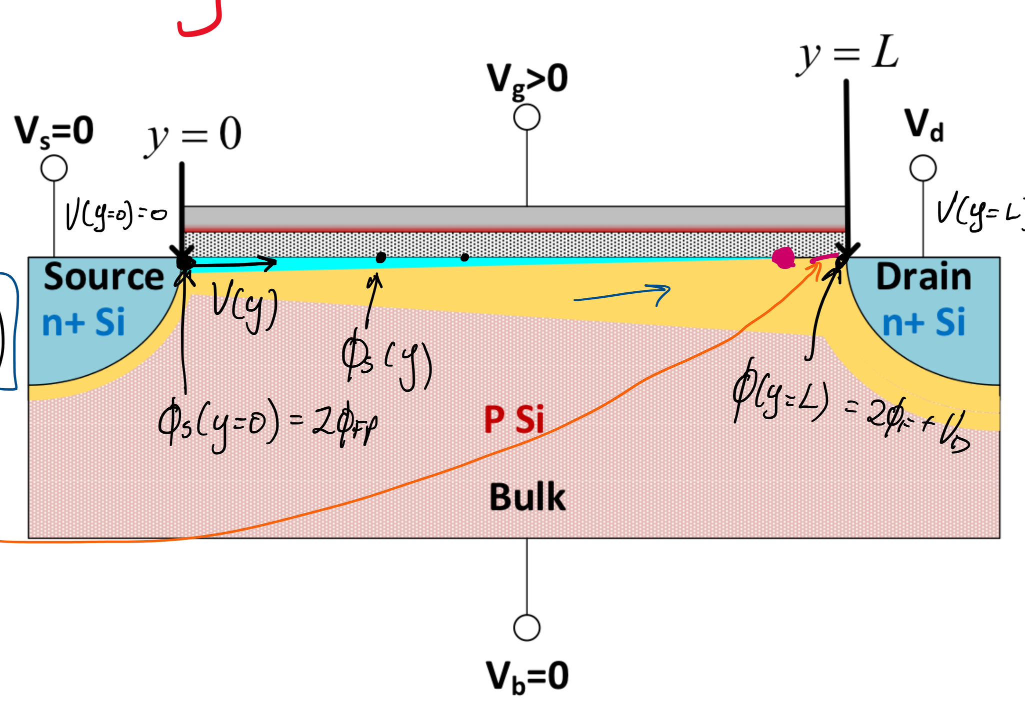
$$\phi_s(y) = 2\phi_F + V(y)$$

- We see it increases along the length of the device
- We know inversion charge is given by:

$$Q_{inv}(y) = -\sqrt{2q\varepsilon_{Si} N_A \phi_s(y)} - C_{ox}(V_G - \phi_s(y))$$

If $\phi_s(y)$ gets Large, $Q_{inv} \mapsto 0$

This Happens Near the drain!



- The Drain Voltage where the Inversion Charge goes to zero is when:

$$* \quad V_D \geq V_G - V_{TO} = V_{DSAT} \quad * \; *$$

- Filling this into the current equation:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left([V_G - V_{TO}]V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right)$$

($[V_G - V_{TO}] = V_{DSAT}$)

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_{DSAT}^2 - \frac{1}{2}V_{DSAT}^2\right)$$

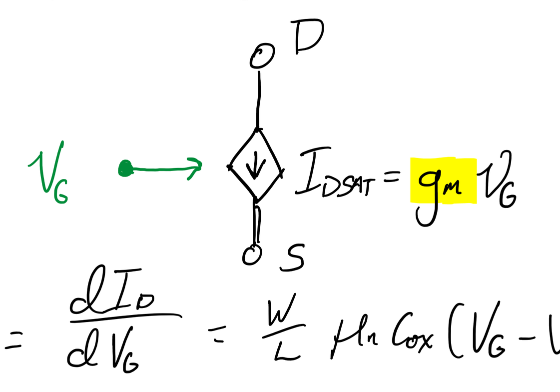
$$= \frac{W}{L}\frac{\mu_n C_{ox}}{2}V_{DSAT}^2$$

- And so the Drain Current in Saturation:

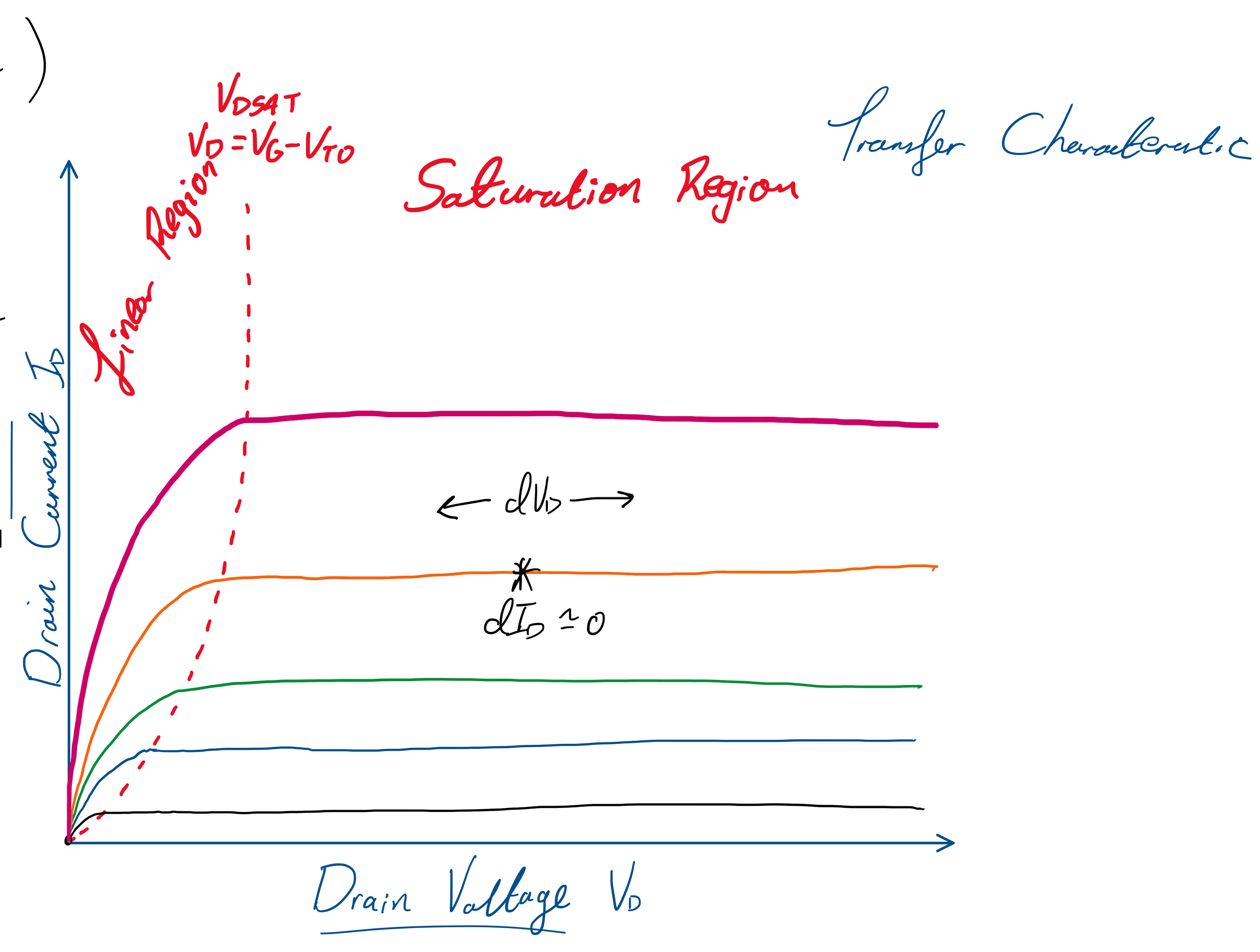
$$I_{DSAT} = \frac{W}{L} \cdot \frac{\mu_n C_{ox}}{2}(V_G - V_{TO})^2$$

Doesn't depend on Drain Voltage!

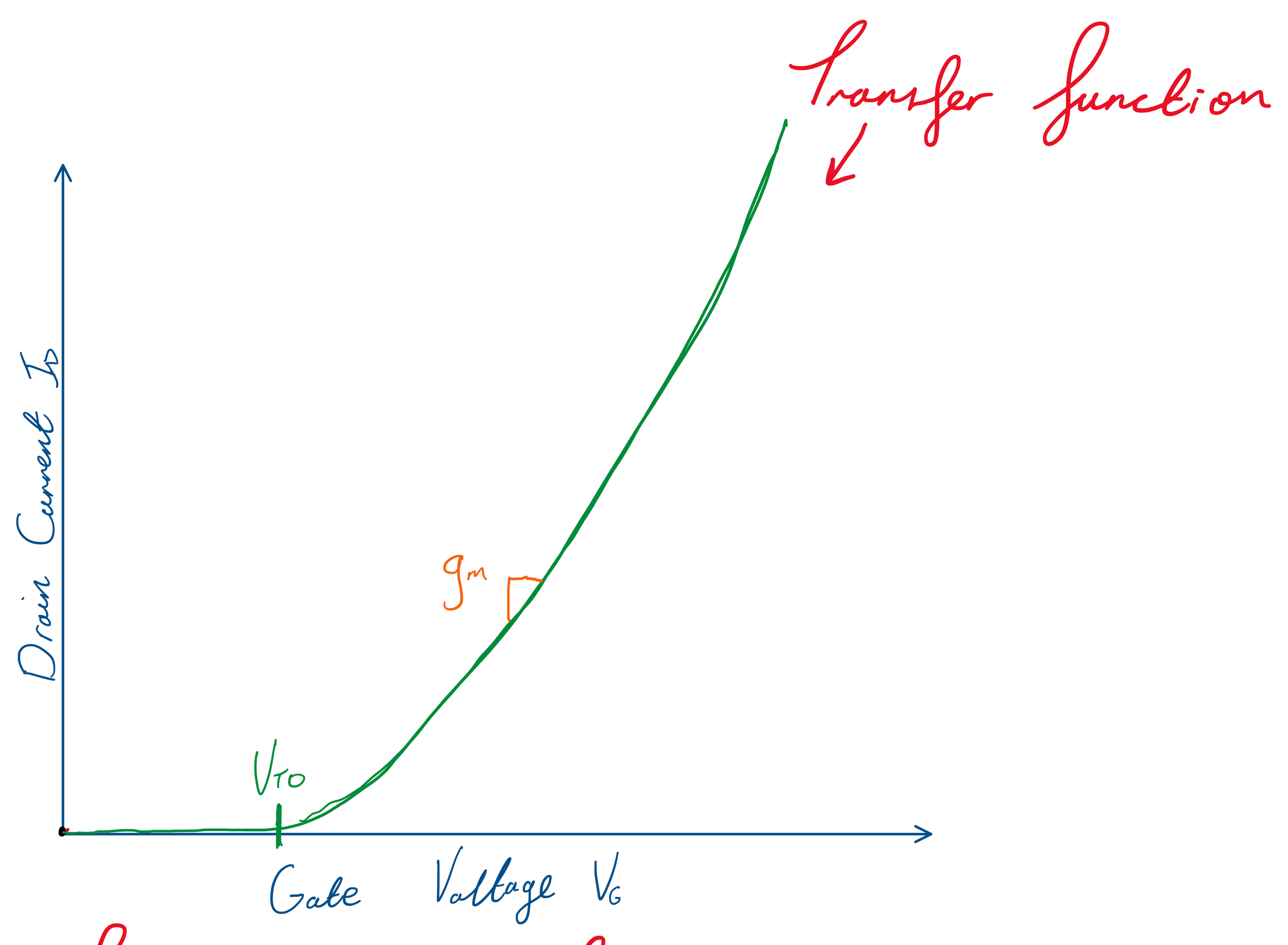
- The MOSFET Looks like a Current Source controlled by the Gate Voltage:



$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L}\mu_n C_{ox}(V_G - V_{TO})$$



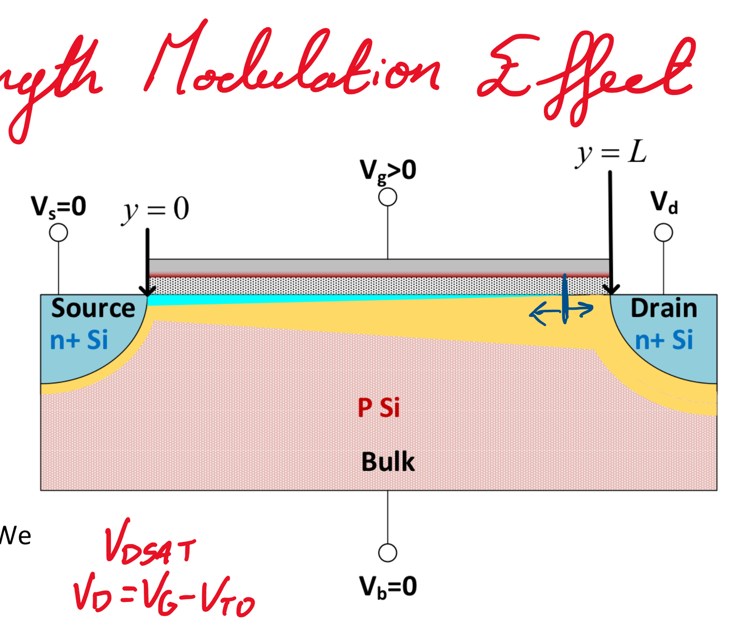
Transfer function



The Channel Length Modulation Effect

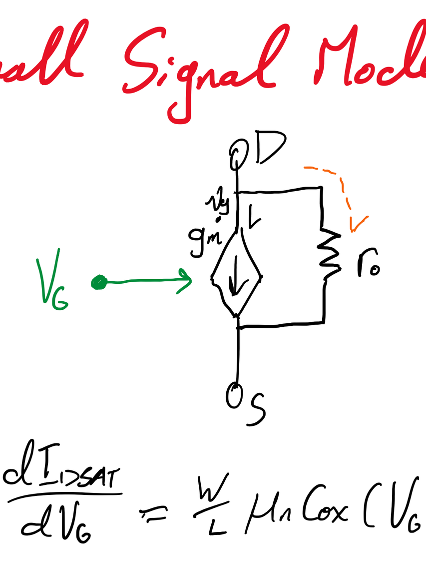
- In real devices, the end of the channel varies slightly with changing Drain Voltage ΔV_D
- This introduces a *slight* dependence on V_D :
- We model this with λ, the channel length modulation parameter:

$$I_{D_{SAT}} \simeq \frac{W}{L}\frac{\mu_n C_{ox}}{2}\left((V_G - V_{TO})^2(1 + \lambda V_D)\right)$$



- The Saturation current now lightly depends on Drain Voltage. We model this as a resistance in series with the controlled current source:

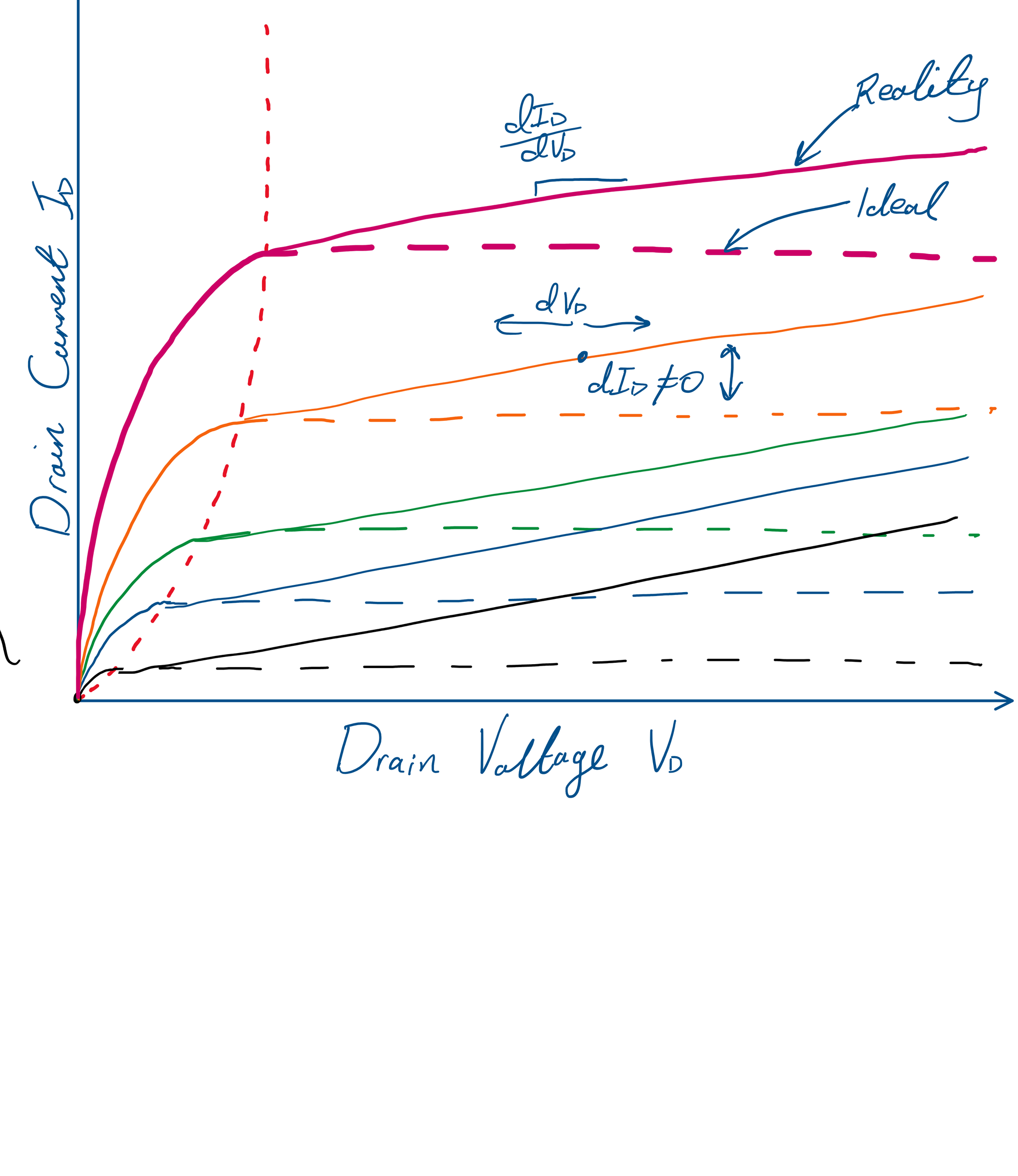
Small Signal Model



$$g_m = \frac{dI_{DSAT}}{dV_G} = \frac{W}{L}\mu_n C_{ox}(V_G - V_{TO})$$

$$\frac{1}{r_o} = \frac{dI_{DSAT}}{dV_D} = \frac{W}{L}\frac{\mu_n C_{ox}}{2}(V_G - V_{TO})^2\lambda$$

$$= \frac{1 + \lambda V_{DS}}{\lambda I_D}$$



Let's Analyse A Real Device

A Standard 65nm device (NMOS Core)

e.g. Intel Core 2 Duo, Xbox 360 Opus CPU, iPhone 3Gs CPU